

FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT					ATTORNEY DOCKET NO.: CDS-008 APPLICANTS: Bellantoni et al. SERIAL NO.: 10/820,459 FILING DATE: 8-Apr-2004 GROUP: 2123				
FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
/HD/	C1	Andrews, J., Axis Systemss Inc., "Co-verification speeds SOC design," EDN, September 5, 2002, pp. 95-96, 98, 100.							
/HD/	C2	Axis Systems, Inc., "Xport™ ARM® Solution," Datasheet, www.AxisSystems.com, 2 pages.							
/HD/	C3	Becker, M., "Faster Verilog Simulations Using a Cycle Based Programming Methodology," <i>Proceedings 1996 IEEE International Verilog HDL Conference</i> , Feb. 26-28, 1996, Santa Clara, CA, USA: IEEE Computer Society Press, 1996, pp. 24-31.							
/HD/	C4	Bell, G., "Solidification - Static Functional Verification with Solidify," HDAG, Inc., 8 pages.							
/HD/	C5	Björklund, D. et al., "A Language for Multiple Models of Computation," <i>Proceedings of the Tenth International Symposium on Hardware/Software Codesign</i> , May 6-8, 2002, Estes Park, CO, USA: CODES 2002, 2002 ACM, pp. 25-30.							
/HD/	C6	Braun, G. et al., "Using Static Scheduling Techniques for the Retargeting of High Speed, Compiled Simulators for Embedded Processors from an Abstract Machine Description," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 57-62.							
/HD/	C7	Chatelain, A. et al., "High-Level Architectural Co-Simulation Using Esterel and C," <i>Proceedings of the Ninth International Workshop on Hardware/Software Codesign/CASHE</i> , April 25-27, 2001, Copenhagen, Denmark: 2001 ACM, pp. 189-194.							
/HD/	C8	Choi, K. et al., "Incremental-in-time algorithm for digital simulation" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 12-15, 1988, <i>Proceedings of the Design Automation Conference</i> . Anaheim (DAC), New York, IEEE, US, vol. CONF. 25, 12-Jun-1988, pages 501-505.							
/HD/	C9	Clarke, P., "Cambridge startup claims speedier simulation tools," <i>EE Times</i> , http://www.eetimes.com/story/OEG2000424S0041 ; April 24, 2000, 2 pages.							
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/HD/	C10	Clarke, P., "EDA tool generates bit- and cycle-accurate C code," <i>EE Times</i> , http://www.eetimes.com/story/OEG20010713S0069 ; July 13, 2001, 1 page.
	C11	Clarke, P., "Tenison tool draws Verilog into SystemC compilation," <i>EEdesign</i> , http://www.eedesign.com/article/showArticle.jhtml?articleID=17406761 ; December 18, 2000, 2 pages.
	C12	Creusillet, B. et al., "Interprocedural analyses of Fortran programs" <i>Parallel Computing</i> , Elsevier Publishers, Amsterdam, NL, vol. 24, no. 3-4, May 1998, pages 629-648.
	C13	DeVane, C. J., "Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits" <i>Computer-Aided Design</i> , 1997. Digest of Technical Papers., 1997 IEEE/ACM International Conference on San Jose, CA, USA 9-13 Nov. 1997.
	C14	Donnelly, K., "High performance VHDL simulation using native compiled code" <i>Electronic Engineering</i> , Morgan-Grampian LTD. London, GB, vol. 65, no. 803, 01-Nov.1993, page 51, 53, 55, 57.
	C15	Duarte, D. et al., "Evaluating the Impact of Architectural-Level Optimizations on Clock Power," <i>Proceedings of the 14th Annual IEEE International ASIC/SOC Conference</i> , Sept. 12-15, 2001, Arlington, VA, USA: 2001 IEEE, pp. 447-451.
	C16	Edwards, C., "Two startups jump into co-verification," <i>EEdesign</i> , http://www.design.com/article/printableArticle.jhtml?articleID=17407943 ; September 23, 2002, 3 pages.
↓	C17	Edwards, C., "U.K.'s Celoxica, Tenison enter co-verification fray," <i>Electronic Engineering Times</i> , October 14, 2002, pp. 24, 27.
/HD/	C18	Edwards, S. A., "Compiling Esterel into sequential code" <i>Proc Des Autom Conf; Proceedings - Design Automation Conference 2000 IEEE</i> , Piscataway, NJ, USA, 2000, pages 322-327.
	C19	French, R.G. et al., "A General Method for Compiling Event-Driven Simulations," Stanford University, http://suif.stanford.edu/papers/rfrench95/paper.html; 19 pages.
	C20	Groves, D., Tenison Technology, "VTOG Verilog → C," <i>International Workshop on Rapid System Prototyping</i>, Tenison TechEDA, www.tenisontech.com, pp. 1-12.
/HD/	C21	Gupta, S. et al., "Conditional Speculation and its Effects on Performance and Area for High-Level Synthesis," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 171-176.
/HD/	C22	Hoffman, A. et al., "A Framework for Fast Hardware-Software Co-simulation," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition 2001</i> , Munich, Germany, March 13-16, 2001. IEEE Computer Society 2001, pp. 760-764.
/HD/	C23	International Search Report PCT/US 03/35649 dated 01-Dec-04
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/HD/	C24	International Search Report PCT/US 03/35403 dated 14-Dec-04
	C25	International Search Report PCT/US 03/35508 dated 05-Jan-05
	C26	Iyer, A. et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," <i>Proceedings of the 29th International Symposium on Computer Architecture (ISCA '02)</i> , May 25-29, 2002, Anchorage, AK, USA: IEEE Computer Society 2002, pp. 158-168.
	C27	Joon-Seo, Yim, et al., "A C-based RTL Design Verification Methodology For Complex Microprocessor" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 9-13, 1997, New York, ACM, IS, vol. CONF. 34, 09-Jun-1997, pages 83-88.
	C28	Ju, Y-C, et al., "Incremental Circuit Simulation Using Waveform Relaxation" <i>Proceedings of the ACM/IEEE Design Automation Conference</i> . Anaheim, June 8-12, 1992, <i>Proceedings of the ACM/IEEE Design Automation Conference (DAC)</i> , Los Alamitos, IEEE Comp. Soc. Press, US, vol. CONF. 29, 08-Jun-1992, pages 8-11.
	C29	Jung, Y. et al., "simCore: an event driven simulation framework for performance evaluation of computer systems" <i>Modeling, analysis and simulation of computers and telecommunication systems</i> , 2000. <i>Proceedings. 8th International Symposium on San Francisco, CA, USA 29 Aug. - 1 Sept. 2002</i> .
	C30	Kim, M.G. et al., "Implementation of a Cycle-Based Simulator for the Design of a Processor Core," <i>Proceedings of AP-ASIC '99: The First IEEE Asia-Pacific Conference on ASICs</i> , Aug. 23-25, 1999, Seoul, South Korea: 1999 IEEE, pp. 108-111.
	C31	Kravitz, S.A. et al., "Massively parallel switch-level simulation : A feasibility study" <i>IEEE Inc.</i> New York, US, vol. 10, no. 7, 01-Jul-97, pages 871-894.
	C32	Krishnaswamy, V. et al., "Parallel Compiled Event Driven VHDL Simulation" <i>Conference Proceedings of the 1998 International Conference on Supercomputing ACM New York, NY, USA, July 1997</i> , pages 297-304.
	C33	Kudlugi, M. et al., "Static Scheduling of Multiple Asynchronous Domains for Functional Verification," <i>DAC 2001</i> , June 18-22, 2001, Las Vegas, Nevada, USA: 2001 ACM, 6 pages.
	C34	Liu, J. et al., "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator," <i>Proceedings of the Sixth International Workshop on Hardware/Software Codesign (CODES/CASHE '98)</i> , March 15-18, 1998, Seattle, Washington, USA: 1998 IEEE, pp. 65-69.
↓	C35	Maurer, P.M., "Scheduling Blocks for Heirarchical Compiled Simulation," Technical Report DA-23, 1991, VCAPP Laboratory, University of South Florida, ftp://pangolin.csee.usf.edu/pub/facul.ty/maurer/tech-reports/da23_91.pdf , 23 pages.
/HD/	C36	McCammon, R. et al., "Cycle-accurate model speeds design," <i>EE Times</i> , http://www.eetimes.com/story/OEG19990615S0021 ; November 13, 2002, 6 pages.
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/HD/	C37	Palnitkar, S. et al., Sun Microsystems, Inc., "Cycle Simulation Techniques," <i>Proceedings of the 1995 IEEE International Verilog HDL Conference</i> , March 27-29, 1995, Santa Cruz, CA, USA: IEEE Computer Society Press, 1995, pp. 2-8.
/HD/	C38	Paul, J.M. et al., "Frequency Interleaving as a Codesign Scheduling Paradigm," <i>Proceedings of the Eighth International Workshop on Hardware/Software Codesign</i> , May 3-5, 2000, San Diego, CA, USA: CODES 2000, ACM 2000, pp. 131-135.
/HD/	C39	Schulz, S.E., "Timing analysis tools in the critical path have a crucial impact on the success of a design," <i>EEDesign</i> , http:// www.eedesign.com/editorial/2000/focusreport0008.html ; November 13, 2002, 6 pages.
/HD/	C40	Stoye, W. et al., "Using Tenison VTOC™ for Large SoC Concurrent Engineering: A Real World Case Study," <i>GlobespanVirata</i> , TenisonEDA, www.tenison.com ; pp. 1-13.
/HD/	C41	Sun Young Hwang, "Incremental algorithms for digital simulation" <i>Integration, The VLSI Journal</i> , North-Holland Publishing Company. Amsterdam, NL, vol. 7, no. 1, 01-Apr-1989, pages 21-34.
/HD/	C42	Tabbara, B. et al., "Fast Hardware-Software Co-Simulation Using VHDL Models," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition</i> , 1999, Munich, Germany, March 9-12, 1999. IEEE Computer Society 1999, pp. 309-316.
	C43	TenisonEDA, "Engineering Management in the SOC Era," www.tenison.com, 1 page.
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/HD/	C45	TenisonEDA, "Introducing VTOC™: Bridging the SOC Co-Development Gap," <i>Tenison EDA World Tour</i> , September 2002, www.tenison.com , 14 pages.
/HD/	C46	TenisonEDA, "VTOC 1.0 User Guide," www.tenison.com ; pp. 1-51.
	C47	Tenison Technology, "A Verilog to C Compiler," <i>Submitted to IEEE Transactions on Software Engineering</i>, pp. 1-10
/HD/	C48	Tenison Technology: Hardware & Software Working Together, "New cycle-based Verilog Compiler is 50 to 100 times faster than behavioural simulation," www.tenisontech.com/news/nw010302.htm ; March 1, 2002, 1 page.
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/HD/	C50	Ye, W. et al., "The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool," <i>Proceedings of the 37th Design Automation Conference</i> , Los Angeles, CA, USA: DAC 2000, 2000 ACM, pp. 340-345.
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